



Atty. Dkt. No. 040301-0487

DIVISION

THE UNITED STATES PATENT AND TRADEMARK OFFICE

2004 JUN 25 PM 2:26

Patentee: Kabushiki Kaisha Toshiba
Title: Semiconductor Integrated Circuit
with Mixed Gate Array and
Standard Cell
Appl. No.: 08/997,035
Patent No. 6,054,872
Issue Date: April 25, 2000

RECEIVED

JUN 28 2004

OFFICE OF PETITIONS

PETITION TO ACCEPT DELAYED PAYMENT OF MAINTENANCE FEE

UNDER SECTION 1.378(c)

Commissioner for Patents – Box Petitions
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

The above-noted patentee, through the undersigned attorney, hereby petitions for acceptance of delayed payment of the first maintenance fee for U.S. Patent No. 6,054,872. The delay in remitting the payment of the maintenance fee due on October 25, 2003 was unintentional. Be advised that Reissue Application No. 09/963,735, filed September 27, 2001, is presently pending before the Patent and Trademark Office, which reissue application corresponds to the captioned U.S. Patent.

The following fees are submitted by check No. 36794, totaling \$2550.00:

1. Required maintenance fee set forth in Sec. 1.20(e) - \$910.00, and
2. Surcharge set forth in Sec. 1.20(i)(2) - \$1640.00.

The Commissioner is hereby authorized to charge any additional fees which may be required regarding this matter under 37 C.F.R. §§ 1.16-1.17, or credit any overpayment, to Deposit Account No. 19-0741. Should no proper payment be enclosed herewith, as by a check being in the wrong amount, unsigned, post-dated, otherwise improper or informal or even entirely missing, the Commissioner is authorized to charge the unpaid amount to Deposit Account No. 19-0741.

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01 FC:1551
02 FC:1558

910.00 OP
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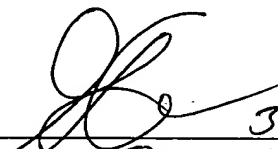
Patentee now awaits confirmation from the U.S. Patent and Trademark Office that the Petition has been granted.

Respectfully submitted,

Date June 24, 2004

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